ABSTRACT

A system in package (SIP) is fabricated on a sheet of copper foil. An interconnection circuit is fabricated on the foil using copper conductors and a dual damascene structure for each conductive layer. The preferred dielectric material is an amorphous fluorinated polymer called Cytop. Input/output traces of the interconnection circuit terminate in wells filled with solder. Chips are bumped and direct attached by inserting the bumps into the wells. The preferred bumps are gold stud bumps, and the preferred wells contain solder paste to a depth of approximately 15 microns. Imprinting is the preferred method for patterning; it enables 6-micron wide traces, 6-micron diameter vias, and a cost per well of around 0.02 cents. Stripline structures are described for a 4-layer stackup that can support operating frequencies of at least 10 GHz. New methods are proposed for testing the completed assembly and for rework of any chips that prove defective. After the assembly is fully tested and reworked in sheet form the copper foil is folded to form a stacked die package or system in package. 5-high and 9-high stacks are illustrated. The copper foil provides a low impedance thermal path for cooling every chip in the SIP.